ABSTRACT OF THE DISCLOSURE

A signal received under a multipath condition is buffered in storage memories 50a and 50b comprising two banks, and while overlap of write and read is allowed,

5   the received data is supplied to matched filters 60a and 60b as much as possible, in a pipeline manner, and in-phase addition of four symbols per unit is performed in in-phase adders 80a and 80b.

In the buffering in storage memories 50a and 50b,

10   processor 40 adaptively changes the search period based on timing information acquired in advance.